5th Semester BE (CBCS) EC Syllabus

Updated on 14-08-17 with

(i) Management and Entrepreneurship – Modification of Title, Some topics according to Text books and Revised Module-5 and (ii) Operating Systems – with more details of Sections of Text Book to be referred (iii) HDL Lab – with tools note

MANAGEMENT AND ENTREPRENEURSHIP DEVELOPMENT

B.E., V Semester, EC/TC/EI/BM/ML

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ES51	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession (Selected topics of Chapter 1, Text 1).

Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making (Selected topics from Chapters 4 & 5, Text 1).

Module-2

Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance**,** Recruitment and Selection Process (Selected topics from Chapters 7, 8 & 11, Text 1).

Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (Selected topics from Chapters 15 to 18 and 9, Text 1).

Module-3

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Selected topics from Chapter 3, Text 1).

Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship (Selected topics from Chapter 2, Text 2).

Module-4

Modern Small Business Enterprises: Role of Small Scale Industries, Impact of Globalization and WTO on SSIs, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Ancillary Industry and Tiny Industry (Definition only) (Selected topics from Chapter1, Text 2).

Institutional Support for Business Enterprises: Introduction, Policies & Schemes of Central Level Institutions, State Level Institutions (Selected topics from Chapter 4, Text 2).

Module-5

Projects Management: A Project. Search for a Business idea**:** Introduction, Choosing an Idea, Selection of product, The Adoption process, Product Innovation, Product Planning and Development Strategy, Product Planning and Development Process. Concepts of Projects and Classification**:** Introduction, Meaning of Projects, Characteristics of a Project, Project Levels, Project Classification, Aspects of a Project, The project Cycle, Features and Phases of Project management, Project Management Processes. Project Identification**:** Feasibility Report, Project Feasibility Analysis. Project Formulation**:** Meaning, Steps in Project formulation, Sequential Stages of Project Formulation, Project Evaluation.

Project Design and Network Analysis: Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.

(Selected topics from Chapters 16 to 20 of Unit 3, Text 3).

Question paper pattern

- The question paper will have TEN questions.
- Each full question carries 16 marks.
- There will be two full questions (with a maximum of Three sub questions) from each module.
- Each full question will have sub questions covering all topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.

Reference Book:

4. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

DIGITAL SIGNAL PROCESSING

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC52	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. Properties of DFT, multiplication of two DFTs- the circular convolution.

Module-2

Additional DFT properties, use of DFT in linear filtering, overlap-save and overlap-add method. Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms).

Module-3

Radix-2 FFT algorithm for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms. Goertzel algorithm, and chirp-z transform.

Module-4

Structure for IIR Systems: Direct form, Cascade form, Parallel form structures.
IIR filter design: Characteristics of commonly used analog filter – Butterworth and Chebyshev filters, analog to analog frequency transformations.
Design of IIR Filters from analog filter using Butterworth filter: Impulse invariance, Bilinear transformation.

Module-5

Structure for FIR Systems: Direct form, Linear Phase, Frequency sampling structure, Lattice structure.
FIR filter design: Introduction to FIR filters, design of FIR filters using - Rectangular, Hamming, Hanning and Bartlett windows.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each

module.

- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. **Digital signal processing – Principles Algorithms & Applications**, Proakis & Monalakis, Pearson education, 4th Edition, New Delhi, 2007.

Reference Books:

1. Discrete Time Signal Processing, Oppenheim & Schaffer, PHI, 2003.
2. Digital Signal Processing, S. K. Mitra, Tata Mc-Graw Hill, 3rd Edition, 2010.
3. Digital Signal Processing, Lee Tan: Elsevier publications, 2007.

Verilog HDL

B.E., V Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC53	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Overview of Digital Design with Verilog HDL

Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. (Text1)

Hierarchical Modeling Concepts

Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text1)

Module-2

Basic Concepts

Lexical conventions, data types, system tasks, compiler directives. (Text1)

Modules and Ports

Module definition, port declaration, connecting ports, hierarchical name referencing. (Text1)

Module-3

Gate-Level Modeling

Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1)

Dataflow Modeling

Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text1)

Module-4

Behavioral Modeling

Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. (Text1)

Module-5

Introduction to VHDL

Introduction: Why use VHDL?, Shortcomings, Using VHDL for Design Synthesis, Design tool flow, Font conventions.

Entities and Architectures: Introduction, A simple design, Design entities, Identifiers, Data objects, Data types, and Attributes. (Text 2)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

2. Kevin Skahill, "**VHDL for Programmable Logic**", PHI/Pearson education, 2006.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

INFORMATION THEORY AND CODING

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC54	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours / Module)	Exam Hours	03
CREDITS – 04			

Modules

Module-1

Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model of Information Sources, Entropy and Information rate of Markoff Sources (Section 4.1, 4.2 of Text 1).

Module-2

Source Coding: Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI (Section 2.2 of Text 2).

Encoding of the Source Output, Shannon's Encoding Algorithm (Sections 4.3, 4.3.1 of Text 1).

Shannon Fano Encoding Algorithm, Huffman codes, Extended Huffman coding, Arithmetic Coding, Lempel – Ziv Algorithm (Sections 3.6,3.7,3.8,3.10 of Text 3).

Module-3

Information Channels: Communication Channels (Section 4.4 of Text 1).

Channel Models, Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies, Mutual Information, Channel Capacity, Channel Capacity of : Binary Symmetric Channel, Binary Erasure Channel, Muroga,s Theorem, Contineuos Channels (Sections 4.2,4.3,4.4,4.6,4.7 of Text 3).

Module-4

Error Control Coding:

Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error Detection and Error Correction Capabilities of Linear Block Codes, Single Error Correcting hamming Codes, Table lookup Decoding using Standard Array.

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction

(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1).

Module-5

Some Important Cyclic Codes: Golay Codes, BCH Codes (Section 8.4 – Article 5 of

Text 2).

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) (Section 8.5 – Articles 1,2 and 3, 8.6- Article 1 of Text 2).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. Digital and analog communication systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.
3. Information Theory and Coding, Muralidhar Kulkarni , K.S. Shivaprakasha, Wiley India Pvt. Ltd, 2015, ISBN:978-81-265-5305-1.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of digital communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, K.N.Hari bhat, D.Ganesh Rao, Cengage Learning, 2017.

NANOELECTRONICS

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC551	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text 1).

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text 1).

Module-3

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. (Text 1).

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text 1).

Module-4

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. (Text 2)

Module-5

Nanosensors: Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smartdust-Sensor for the future. (Text 3)

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.
3. T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH.

Reference Books:

1. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

SWITCHING & FINITE AUTOMATA THEORY

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC552	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Threshold Logic: Introductory Concepts: Threshold element, capabilities and limitations of threshold logic, Elementary Properties, Synthesis of Threshold networks: Unate functions, Identification and realization of threshold functions, The map as a tool in synthesizing threshold networks. (Sections 7.1, 7.2 of Text)

Module-2

Reliable Design and Fault Diagnosis: Hazards, static hazards, Design of Hazard-free Switching Circuits, Fault detection in combinational circuits, Fault detection in combinational circuits: The faults, The Fault Table, Covering the fault table, Fault location experiments: Preset experiments, Adaptive experiments, Boolean differences, Fault detection by path sensitizing. (Sections 8.1, 8.2, 8.3, 8.4, 8.5 of Text)

Module-3

Sequential Machines: Capabilities, Minimization and Transformation

The Finite state model and definitions, capabilities and limitations of finite state machines, State equivalence and machine minimization: k-equivalence, The minimization Procedure, Machine equivalence, Simplification of incompletely specified machines. (Section 10.1, 10.2, 10.3, 10.4 of Text)

Module-4

Structure of Sequential Machines: Introductory example, State assignment using partitions: closed partitions, The lattice of closed partitions, Reduction of output dependency, Input dependence and autonomous clocks, Covers and generation of closed partitions by state splitting: Covers, The implication graph, An application of state splitting to parallel decomposition. (Section 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 of Text)

Module-5

State–Identification and Fault Detection Experiments: Experiments, Homing experiments, Distinguishing experiments, Machine identification, Fault detection experiments, Design of diagnosable machines, Second algorithm for the design of fault detection experiments. (Sections 13.1, 13.2, 13.3, 13.4, 13.5, 13.6, 13.7 of Text)

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**

- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

Switching and Finite Automata Theory - Zvi Kohavi, McGraw Hill, 2nd edition, 2010 ISBN: 0070993874.

Reference Books:

1. **Fault Tolerant And Fault Testable Hardware Design**- Parag K Lala, Prentice Hall Inc. 1985.
2. **Digital Circuits and Logic Design**.-Charles Roth Jr, Larry L. Kinney, Cengage Learning, 2014, ISBN: 978-1-133-62847-7.

OPERATING SYSTEM

B.E., V Semester, Electronics & Communication Engineering / Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC553	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Module-1

Introduction to Operating Systems
OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems (Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).

Module-2

Process Management: OS View of Processes, PCB, Fundamental State Transitions, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Long term, medium term and short term scheduling in a time sharing system (Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , 4.2, 4.3, 4.4.1 of Text).

Module-3

Memory Management: Contiguous Memory allocation, Non-Contiguos Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, Paging Hardware, VM handler, FIFO, LRU page replacement policies (Topics from Sections 5.5 to 5.9, 6.1 to 6.3, except Optimal policy and 6.3.1 of Text).

Module-4

File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access (Topics from Sections 7.1 to 7.8 of Text).

Module-5

Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Resource state modelling, Deadlock detection algorithm, Deadlock Prevention (Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**

- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

Operating Systems – A concept based approach, by Dhamdare, TMH, 2nd edition.

Reference Books:

1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.

ELECTRICAL ENGINEERING MATERIALS

B.E., V Semester, Electronics & Communication Engineering/ Telecommunication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC554	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours/Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

Band Theory of Solids: Introduction to free electron theory, Kroning-Penney Model, Explanation for Discontinuities in E vs. K curve, Formation of Solid Material, Formation of Band in Metals, Formation of Bands in Semiconductors and Insulating Materials, Classification of Materials on the Basis of Band Structure, Explanation for differences in the Electrical properties of different Materials. Important Characteristics of a Band Electron, Number of energy states per band, Explanation for Insulating and Metallic Behavior of Materials, Concept of Hole.

Module-2

Magnetic Properties of Materials: Introduction, Origin of Magnetism, Basic Terms in Magnetism, Relation between Magnetic Permeability and Susceptibility, Classification of magnetic Materials, Characteristics of Diamagnetic Materials, Paramagnetic Materials, Ferromagnetic Materials, Ferrimagnetic Materials, Langevin's Theory of Diamagnetism, Explanation of Dia, Para and Ferromagnetism, Ampere's Lam in Dia, Para and Ferromagnetism, Hystersis and Hystersis loss, Langevin's Theory of paramagnetism, Modification in the Langevin's Theory, Anti-Ferromagnetism and Neel Temperature, Ferrimagnetic Materials, Properties of some important Magnetic Materials, Magentostriction and Magnetostrictive Materials, Hard and Soft Ferromagnetic Materials and their Applications.

Module-3

Behavior of Dielectric Materials in AC and DC Fields: Introduction, Classification of Dielectric Materials at Microscopic level, Polar Dielectric Materials, Non-polar Dielectric Materials, Kinds of Polarizations, behavior of dielectric materials, Three electric Vectors, Gauss's Law in a Dielectric, Electric Susceptibility and Static Dielectric constant, Effect of Dielectric medium upon capacitance, macroscopic electric field, Microscopic Electric field, temperature dependence of dielectric constant, polar dielectric in ac and dc fields, behavior of polar dielectric at high frequencies, Dielectric loss, Dielectric strength and Dielectric Breakdown, Various kinds of Dielectric Materials, Hysteresis in Ferroelectric Materials, Applications of Ferroelectric Materials in Devices.

Module-4

Conductivity of Metals and Superconductivity: Introduction, Ohm's law, Explanation for the dependence of electrical resistivity upon temperature, Free-electron theory of metals, Application of Lorentz-Drude free-electron theory, Effect of various parameters on Electrical Conductivity, Resistivity Ratio, Variation of resistivity of alloys with temperature, Thermal Conductivity of Materials, Heat produced in Current Carrying Conductor, Thermoelectric Effect, Thermoelectric Series, Seebeck's Experiment.

Discovery of superconductivity, superconductivity and transition temperature, superconducting materials, explanation of superconductivity phenomenon, characteristics of superconductors, change in thermodynamic parameters in superconducting state, frequency dependence of superconductivity, current status of high temperature superconductors, practical applications of superconductors.

Module-5

Electrical Conducting and Insulating materials: Introduction, Classification of conducting materials, difference in properties of Hard-Drawn and Annealed copper, standard conductors, comparison between some popular Low-Resistivity Materials, Low-Resistivity Copper Alloys, Electrical contact materials and their selection, classification of contact materials, Materials for Lamp Filaments, Preparation of Tungsten Filaments.

Insulating gases, Liquids and solids and their characteristics, Selection of the insulating material, other important properties of Insulating materials, Thermal characteristics , chemical properties of Insulating materials, classification of Insulating materials on the basis of structure.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

1. R K Shukla and Archana Singh, "Electrical Engineering Materials" McGraw Hill, 2012, ISBN: 978-1-25-90062-03.

Reference Books:

1. S.O. KASAP, "Electronic Materials and Devices" 3rd edition, McGraw Hill, 2014, ISBN-978-0-07-064820-3.
2. C.S.Indulkar and S. Thiruvengadam, S., "An Introduction to Electrical Engineering Materials", ISBN-9788121906661.

MSP430 MICROCONTROLLER

B.E., V Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15EC555	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03
CREDITS – 03			

Modules

Module-1

MSP430 Architecture: Introduction – Where does the MSP430 fit, The outside view, The inside view-Functional block diagram, Memory, Central Processing Unit, Memory Mapped Input and Output, Clock Generator, Exceptions: Interrupts and Resets, MSP430 family.
(Text: Ch1- 1.3 to 1.7, Ch2- 2.1 to 2.7, Ch5- 5.1, 5.7 upto 5.7.1)

Module-2

Addressing Modes & Instruction Set- Addressing Modes, Instruction set**,** Constant Generator and Emulated Instructions, Program Examples.
(Text: Ch5- 5.2 to 5.5)

Module-3

Clock System, Interrupts and Operating Modes- Clock System, Interrupts, What happens when an interrupted is requested, Interrupt Service Routines, Low Power Modes of Operation, Watchdog Timer, Basic Timer1, Real Time Clock, Timer-A: Timer Block, Capture/Compare Channels, Interrupts from Timer-A.
(Text: Ch5 - 5.8 upto 5.8.4, Ch 6-6.6 to 6.8, 6.10, Ch8 -8.1, 8.2, 8.3)

Module-4

Analog Input-Output and PWM - Comparator-A, ADC10, ADC12, Sigma-Delta ADC, Internal Operational Amplifiers, DAC, Edge Aligned PWM, Simple PWM, Design of PWM. LCD interfacing.
(Text: Ch9 – 9.1 upto 9.1.2, 9.4, 9.5 upto 9.5.1, 9.7, 9.8 upto 9.8.1, 9.11.5, 9.12 (without 9.12.1), 8.6.2 to 8.6.4)

Module-5

Digital Input-Output and Serial Communication:
Parallel Ports, Lighting LEDs, Flashing LEDs, Read Input from a Switch, Toggle the LED state by pressing the push button, LCD interfacing.
Asynchronous Serial Communication, Asynchronous Communication with USCI_A, Communications, Peripherals in MSP430, Serial Peripheral Interface.
(Text: Selected topics from Ch4 & Ch7 and Ch7- 7.1, Ch10 – 10.1, 10.2, and 10.12)

Evaluation of Internal Assessment Marks:

It is suggested that at least a few simple programs to be executed by students using any evaluation board of MSP430 for better understanding of the course. This activity can be considered for the evaluation of 5 marks out of 20 Internal assessment marks, reserved for the other activities.

Question paper pattern:

- The question paper will have ten questions
- Each full question consists of 16 marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module

Text Book:

John H Davies, MSP430 Microcontroller Basics, Newnes Publications, Elsevier, 2008.

References:

1. Chris Nagy, Embedded Systems Design using TI MSP430 Series, Newnes Publications, Elsevier, 2003.
2. User Guide from Texas Instruments.

DSP Lab

B.E., V Semester, EC/TC

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL57	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory=03	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem.
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parsevals theorem, etc.) (ii) DFT computation of square pulse and Sinc function etc.
7. Design and implementation of FIR filter to meet given specifications (using different window techniques).
8. Design and implementation of IIR filter to meet given specifications.

Following Experiments to be done using DSP kit

9. Linear convolution of two sequences
10. Circular convolution of two sequences
11. N-point DFT of a given sequence
12. Impulse response of first order and second order system
13. Implementation of FIR filter

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

HDL Lab

B.E., V Semester, EC/TC

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	15ECL58	IA Marks	20
Number of Lecture Hours/Week	01 Hr Tutorial (Instructions) + 02 Hours Laboratory = 03	Exam Marks	80
		Exam Hours	03

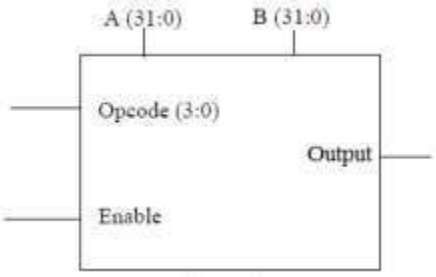
CREDITS – 02

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

Laboratory Experiments

Part–A: PROGRAMMING

1. Write Verilog code to realize all the logic gates
2. Write a Verilog program for the following combinational designs
   a. 2 to 4 decoder
   b. 8 to 3 (encoder without priority & with priority)
   c. 8 to 1 multiplexer.
   d. 4 bit binary to gray converter
   e. Multiplexer, de-multiplexer, comparator.
3. Write a VHDL and Verilog code to describe the functions of a Full Adder using three modeling styles.
4. Write a Verilog code to model 32 bit ALU using the schematic diagram shown below



- ALU should use combinational logic to calculate an output based on the four bit op-code input.
- ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.
- ALU should decode the 4 bit op-code according to the example given below.

OPCODE	ALU Operation
1.	A+B
2.	A-B
3.	A Complement
4.	A*B
5.	A AND B
6.	A OR B
7.	A NAND B
8.	A XOR B

5. Develop the Verilog code for the following flip-flops, SR, D, JK and T.
6. Design a 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.

Part–B: INTERFACING (at least four of the following must be covered using VHDL/Verilog)

1. Write HDL code to display messages on an alpha numeric LCD display.
2. Write HDL code to interface Hex key pad and display the key code on seven segment display.
3. Write HDL code to control speed, direction of DC and Stepper motor.
4. Write HDL code to accept Analog signal, Temperature sensor and display the data on LCD or Seven segment display.
5. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC - change the frequency.
6. Write HDL code to simulate Elevator operation.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.